Amendments to the Specification:

Please replace paragraph [0021] of the specification with the following amended paragraph:

Please refer to Fig.4, which is a circuit diagram of the mirror ratio controller 76 shown in Fig.3. The mirror ration controller 76 has a plurality of mirror ratio setting units 88a, 88b, 88c. Please note that only three mirror ratio setting units are shown for simplicity. When the mirror ratio controller 76 is enabled, the mirror ratio setting units 88a, 88b, 88c function as current dividers for adjusting the current [[Iref]] <u>Iref'</u> that actually passes the transistor 82. Because the reference current Iref is viewed as a current source, the magnitude of the reference current [[Iref]] <u>Iref'</u> becomes less when more current dividers are activated. Taking the mirror ratio setting unit 88a for example, it includes transistors 90a, 91a, 92a, 93a. The transistors 90a, 91a are a PMOS transistor and an NMOS transistor respectively. If a control bit C_0 corresponds to the logic value "1", the transistor switch built by the transistors 90a, 91a is switched on for connecting gates of the transistors 82, 93a. However, the transistor 92a is still turned off. With an adequate reference voltage Vref, the transistor 82 enters a saturation state. Please note that the drain, the source, and the gate of the transistor 93a are respectively connected to the drain, the source, and the gate of the transistor 82. Therefore, the transistor 93a enters the saturation state as well. If the W/L ration is K times as great as the W/L ration of the transistor 82, the reference current [[Iref]] <u>Iref'</u> passing the transistor 82 becomes [1/(1+K)]*Iref. On the contrary, if the control bit C_0 corresponds to another logic value "0", the transistor switch built by the transistors 90a, 91a is not turned on. As this time, the transistor 92a is turned on so that the gate of the transistor 93a approaches a high voltage level Vdd. Therefore, the transistor 93a is turned off, and the reference current [[Iref]] <u>Iref'</u> equals the reference current Iref.

Please replace paragraph [0022] of the specification with the following amended paragraph:

Regarding the mirror ratio setting unit 88b, the operation of the mirror ratio setting unit 88b is similar to that of the mirror ratio setting unit 88a mentioned above. If a

control bit C_1 corresponds to the logic value “1”, and the W/L ratio of the transistor 93b is 2*K times as great as the W/L ratio of the transistor 82, the reference current [[Iref]] Iref’ passing the transistor 82 becomes [1/(1+2*K)]*Iref. On the contrary, if the control bit C_1 corresponds to the logic value “0”, the reference current [[Iref]] Iref’ is equal to the reference current Iref. Therefore, suppose that the mirror ratio controller 76 comprises m mirror ratio setting units, the control bits $C_0, C_1, \ldots\ldots, C_{m-1}$ are used to control magnitude of the reference current [[Iref]] Iref’, and the W/L ratios of the transistors (transistors 93a, 93b for example) are $K*2^T$ ($0 \leqq T \leqq m-1$) times as great as the W/L ratio of the transistor 82 respectively. For instance, the transistor 93a corresponding to the control bit C_0 has a W/L ratio that is $K*2^0$ times as great as the W/L ratio of the transistor 82, the transistor 93b corresponding to the control bit C_1 has a W/L ratio that is $K*2^1$ times as great as the W/L ratio of the transistor 82, and the transistor 93c corresponding to the control bit C_{m-1} has a W/L ratio that is $K*2^{m-1}$ times as great as the W/L ratio of the transistor 82. According to the prior art superposition principle, the reference current [[Iref]] Iref’ is expressed as follows:

[[Iref]]

$$\text{Iref'} = \frac{Iref}{1 + K * C_0 + 2^1 * K * C_1 + \ldots\ldots + 2^{(m-1)} * K * C_{(m-1)}} \qquad \text{Equation (2)}$$

Please replace paragraph [0023] of the specification with the following amended paragraph:

When the voltage calibration circuit 68 is taken into consideration, the reference current [[Iref]] Iref’ expressed by the equation (2) substitutes for the reference current Iref in the equation (1). The output current Iout actually generated from the DAC 66 is described as follows:

$$\text{Iout} = (2^{n-1}*L*D_{n-1} + 2^{n-2}*L*D_{n-2} + \ldots\ldots + 2^0*L*D_0) * \frac{1}{1 + K * C_0 + 2^1 * K * C_1 + \ldots\ldots + 2^{(m-1)} * K * C_{(m-1)}} * Iref \qquad \text{Equation (3)}$$

Please replace paragraph [0032] of the specification with the following amended paragraph:

Generally speaking, the state machine 78 is built by a plurality of flip-flops. After the state machine 96 enters the operational state 96, the state machine, therefore, stops flip-flops from being triggered to achieve the objective of holding the setting value SET. When the DAC 66 starts converting the digital display data into analog display driving voltages, the setting value SET controls the mirror ratio 76 to adjust the display driving voltages corresponding to different gray levels. In the preferred embodiment, the mirror ratio setting units 88a, 88b, 88c of the mirror ratio controller 76 respectively correspond to different W/L ratios. Therefore, the mirror ratio setting units 88a, 88b, 88c have different adjustment magnitude for the reference current [[Iref]] Iref'. However, the mirror ratio setting units 88a, 88b, 88c are capable of having the same W/L ratio for tuning the reference current [[Iref]] Iref'. That is, the total number of the selected mirror ratio setting units dominates the reference current [[Iref]] Iref'. Therefore, more mirror ratio setting units are increased to lower the reference current [[Iref]] Iref' when the setting value SET is increased, and fewer mirror ratio setting units are decreased to boost the reference current [[Iref]] Iref' when the setting value SET is decreased.